

THALES

Time4Sys - Integrating Temporal Performance Verification in your Engineering Practices

WARUNA PROJECT PARTNERS:

INRIA

RT@W

ARTAL

CLEARSY

LIAS


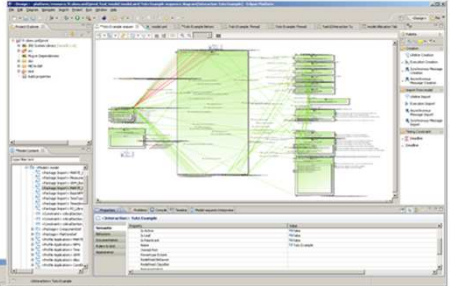
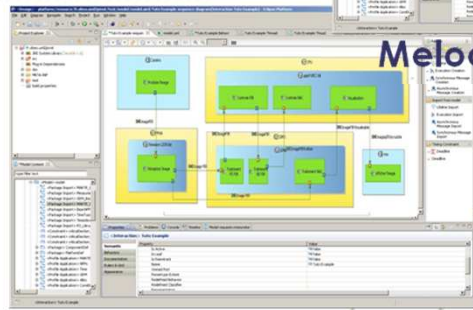
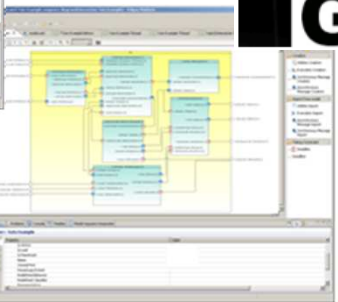
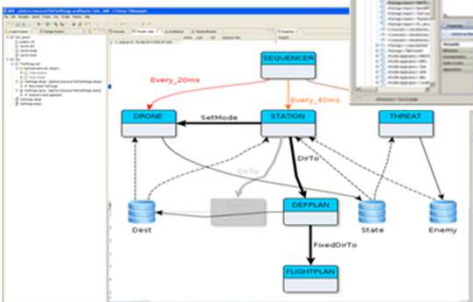
THALES (RAFIK HENIA)

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How can industry Benefit from existing scheduling verification techniques/tools ?

Various design tools

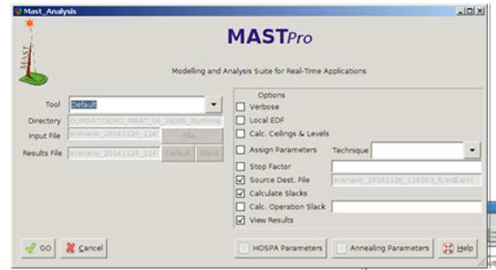
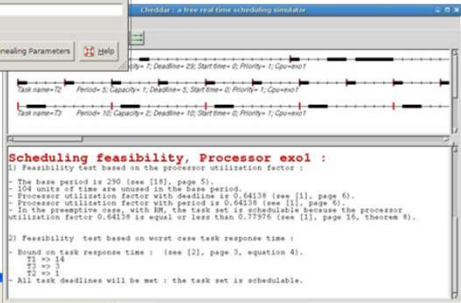
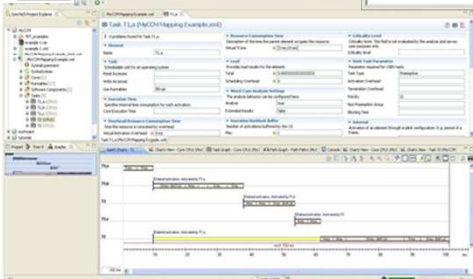
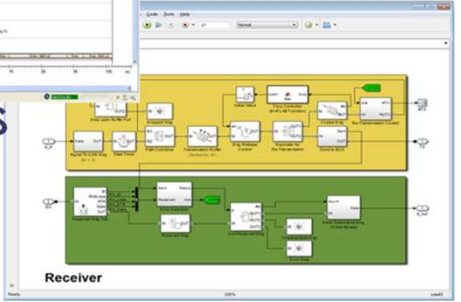
MelodyCCM Spatial

Capella

MelodyCCM

SoftArc

Various timing verification tools

MAST

Cheddar

SymTA/S

Receiver

SimEvents

Scheduling feasibility, Processor exol1 :

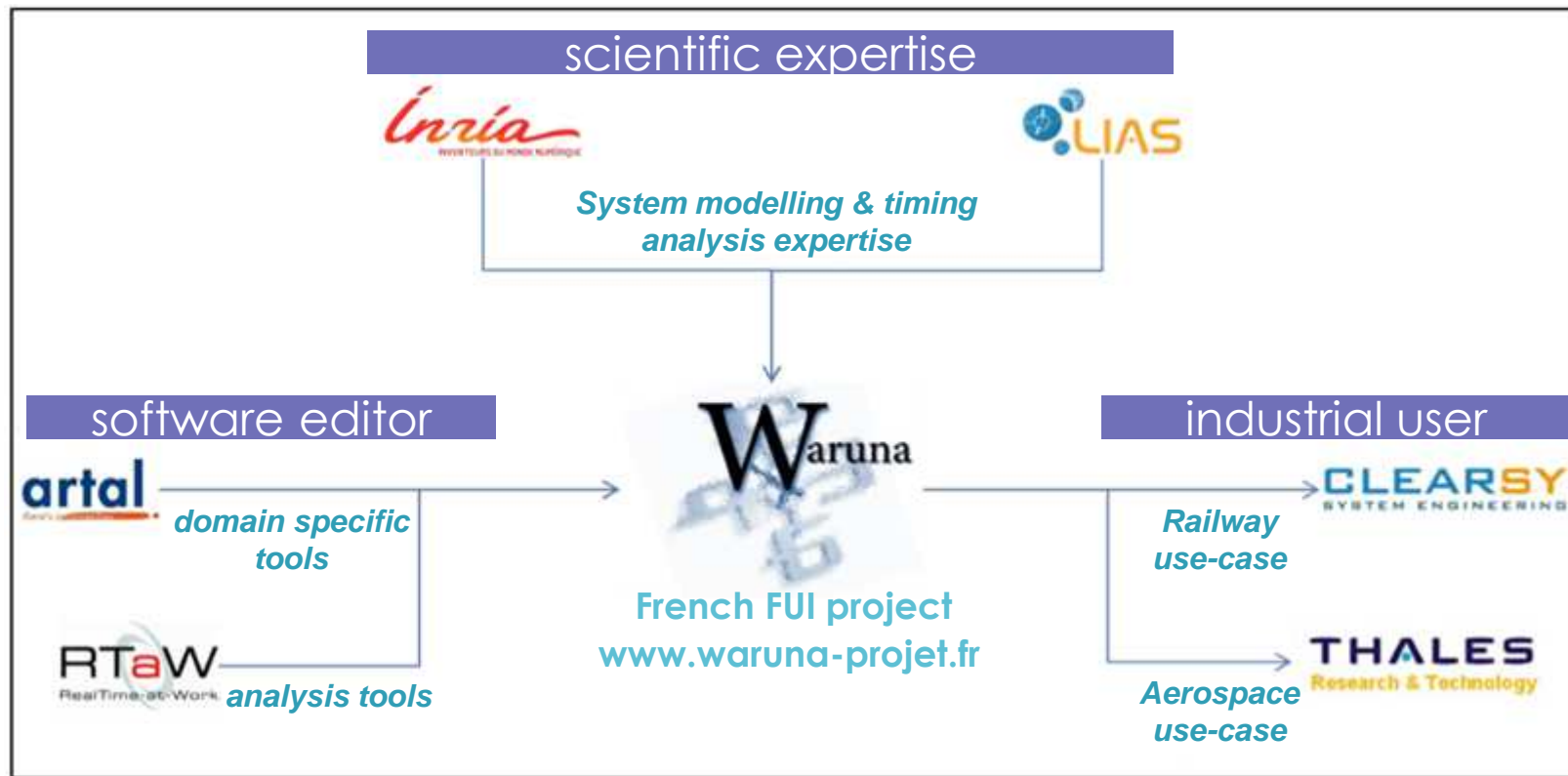
- 1) Feasibility test based on the processor utilisation factor :
 - The base period is 230 (see [1], page 5).
 - 104 units of time are unused in the base period.
 - Processor utilisation factor with deadline is 0.64138 (see [1], page 6).
 - Processor utilisation factor with period is 0.64138 (see [1], page 6).
 - In the progressive case, with RR, the task set is schedulable because the processor utilisation factor 0.64138 is equal or less than 0.79796 (see [1], page 16, theorem 8).
- 2) Feasibility test based on worst case task response time :
 - Bound on task response time : (see [2], page 3, equation 4).
 - $R_1 \leq 14$
 - $R_2 \leq 1$
 - All task deadlines will be met : the task set is schedulable.

G A P

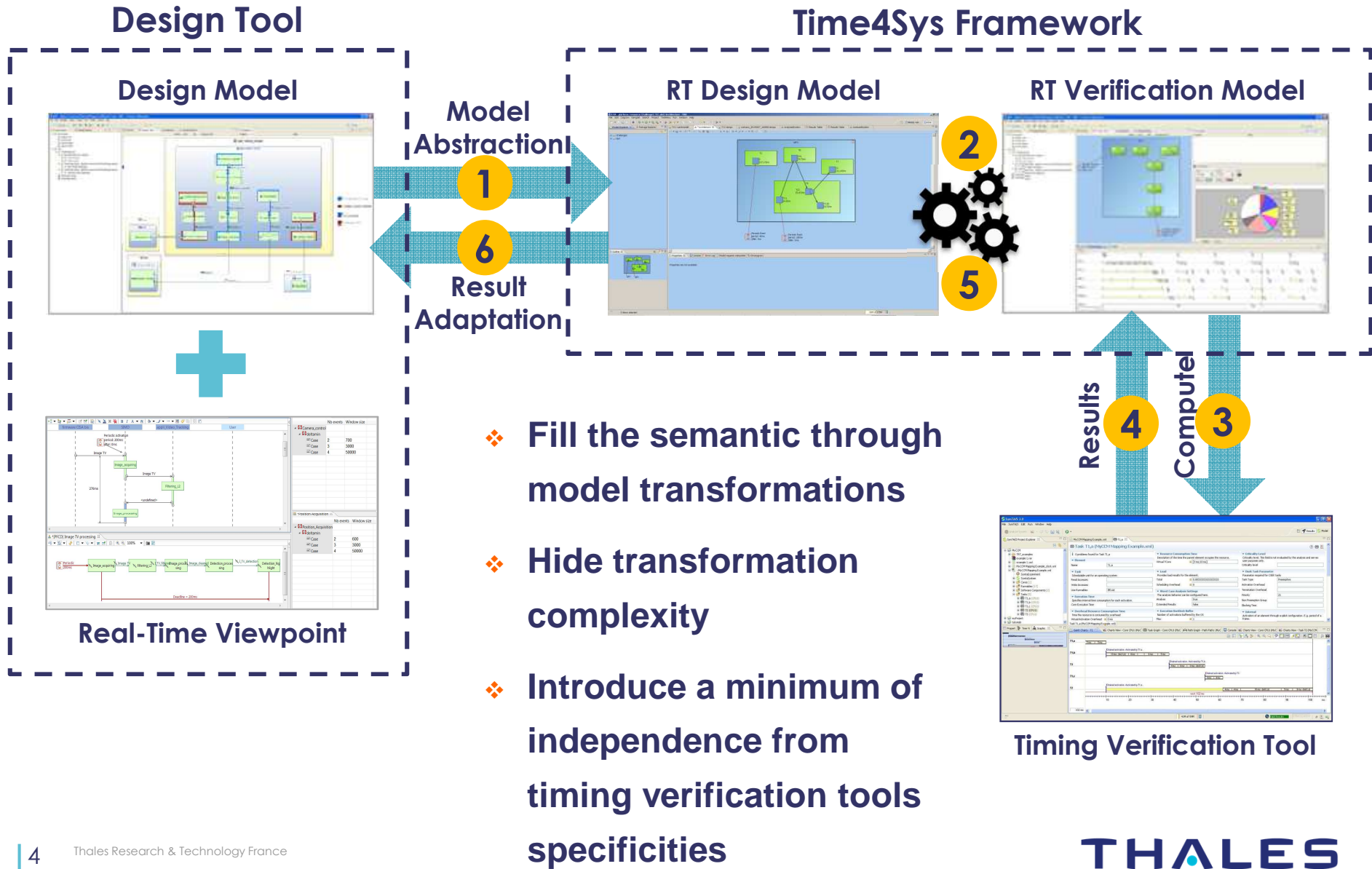
WARUNA project objectives

O1: Develop a modelling framework allowing to perform model-based scheduling verification of real-time systems at early design stages

O2: Reach TRL6 at the end of the project by validating the developed framework on representative industrial use-cases



Connecting design activities to timing performance verification via Time4Sys



Time4Sys Architecture

